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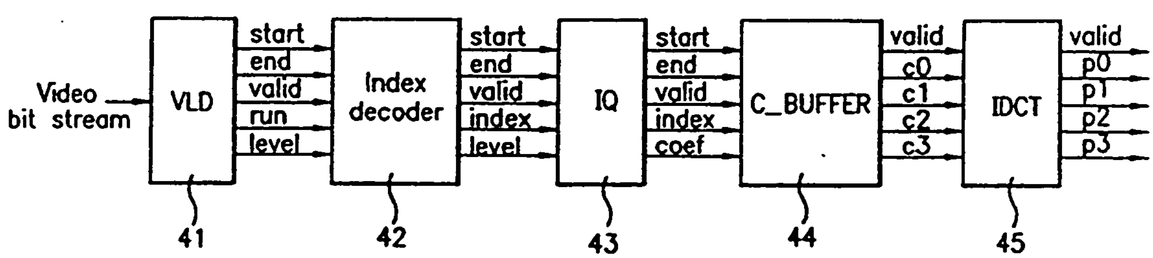
(54) Abstract Title
Video decoder for high picture quality

(57) A video decoder for high definition television includes a variable length decoder 41 decoding codes corresponding to discrete cosine transform (DCT) coefficients of an applied video bit stream, and producing a run-level pair for each code; an index decoder 42 storing run-level pairs produced from the variable length decoder, and producing position information indicating the position of a level value of a corresponding run-level pair; an inverse quantizer 43; an inverse scanner 44 including a plurality of memories, and producing the DCT coefficients in parallel; and an inverse discrete cosine transformer 45.

FIG.4



GB 2 333 201 A

FIG.1
Conventional Art

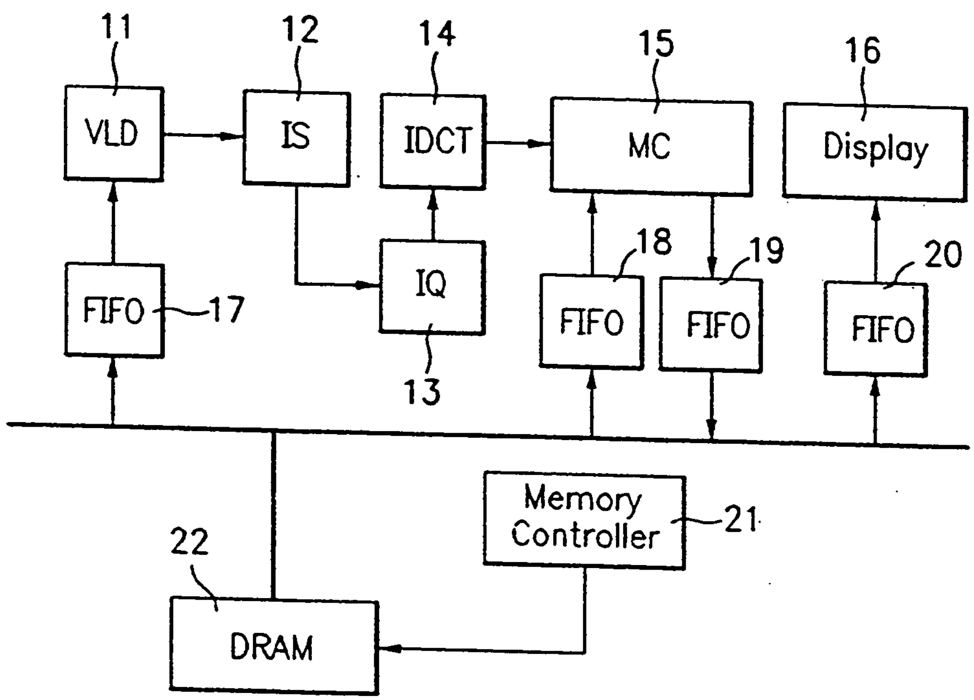


FIG.2
Conventional Art

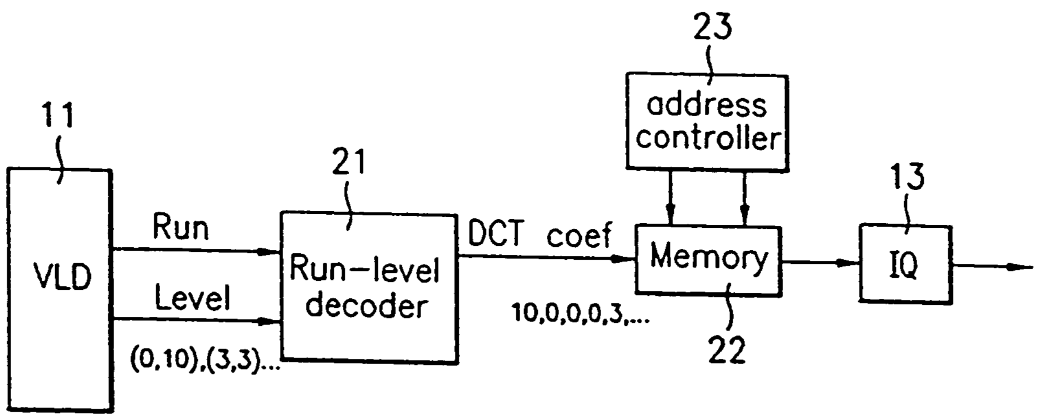


FIG.3A
Conventional Art

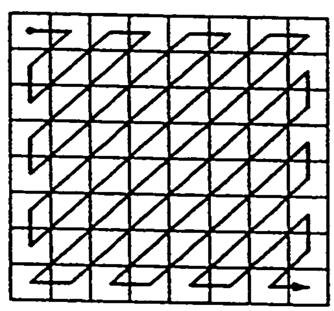


FIG.3B
Conventional Art

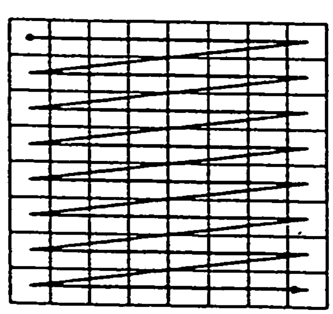


FIG.4

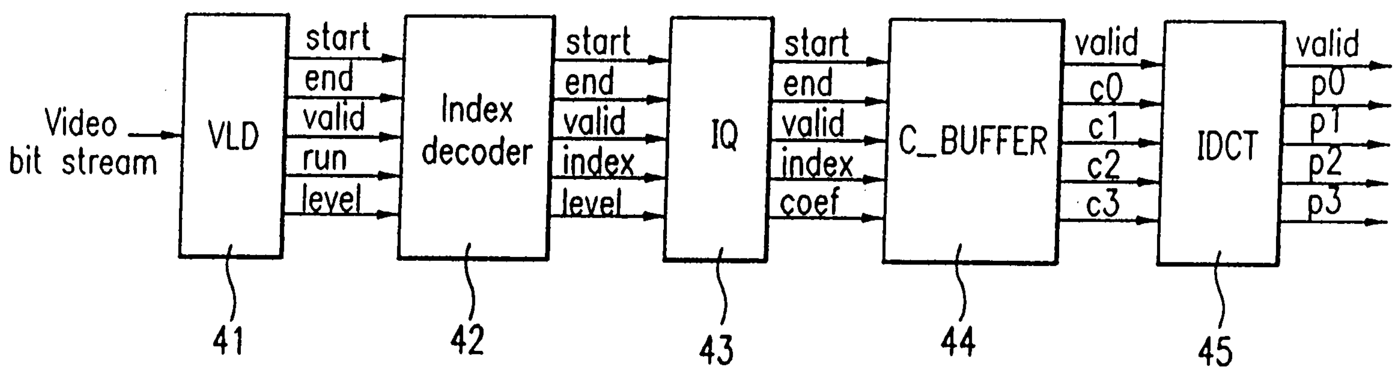

Video bit stream
VLD
start
end
valid
run
level
Index decoder
start
end
valid
index
level
IQ
start
end
valid
index
coef
C_BUFFER
valid
c0
c1
c2
c3
IDCT
valid
p0
p1
p2
p3
41
42
43
44
45

FIG.5

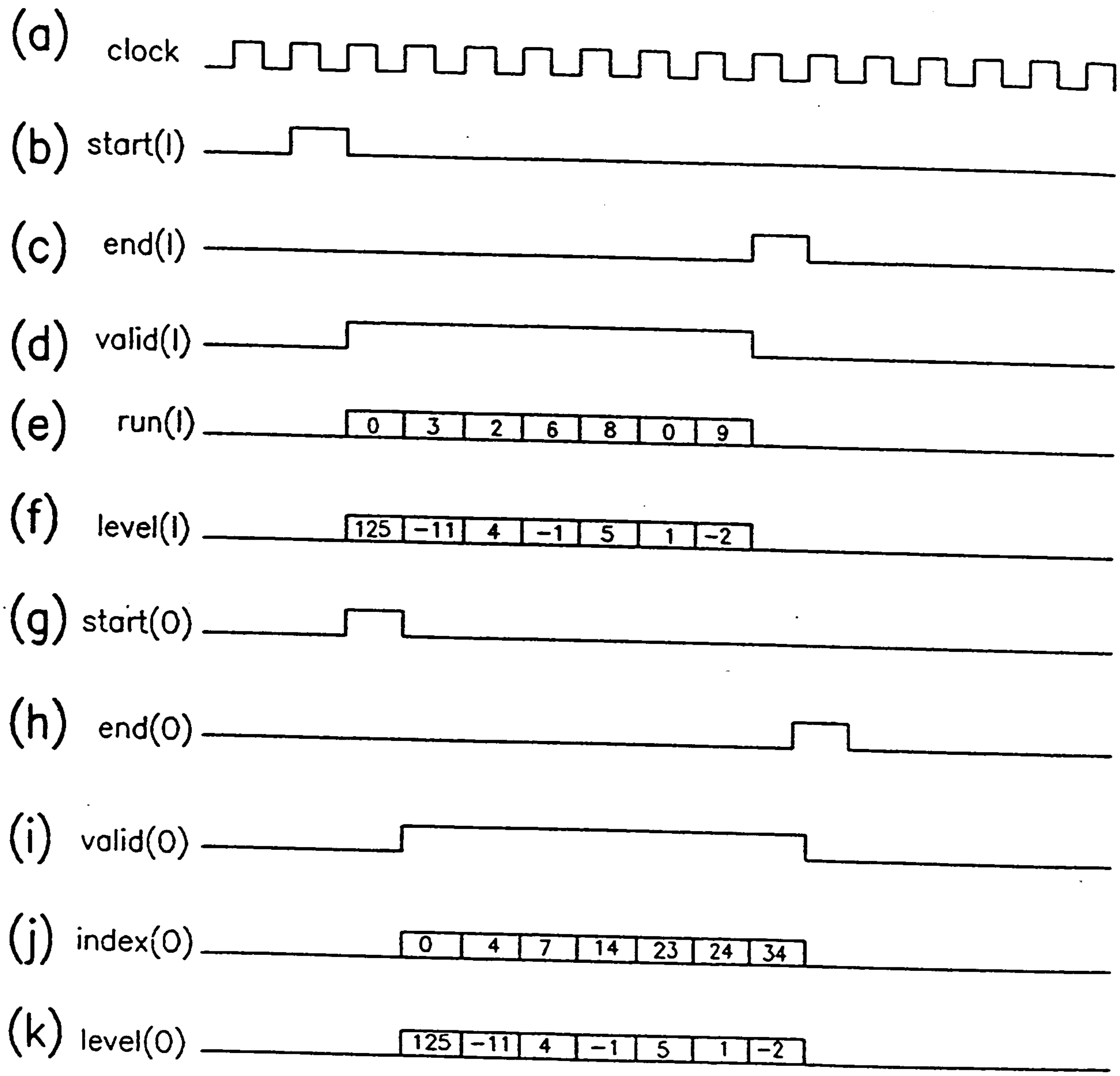
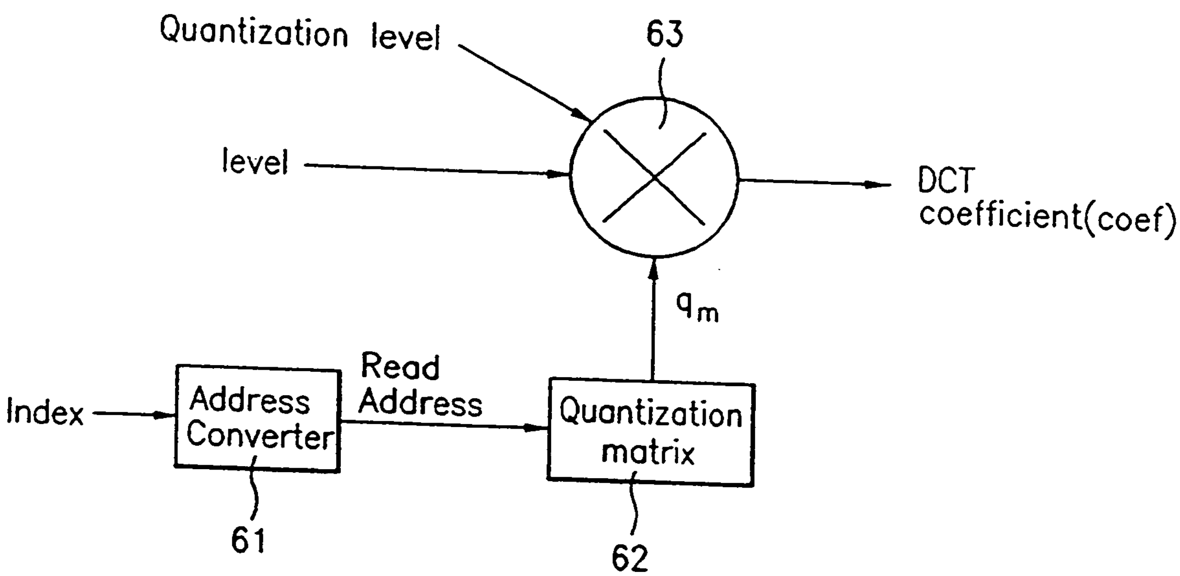
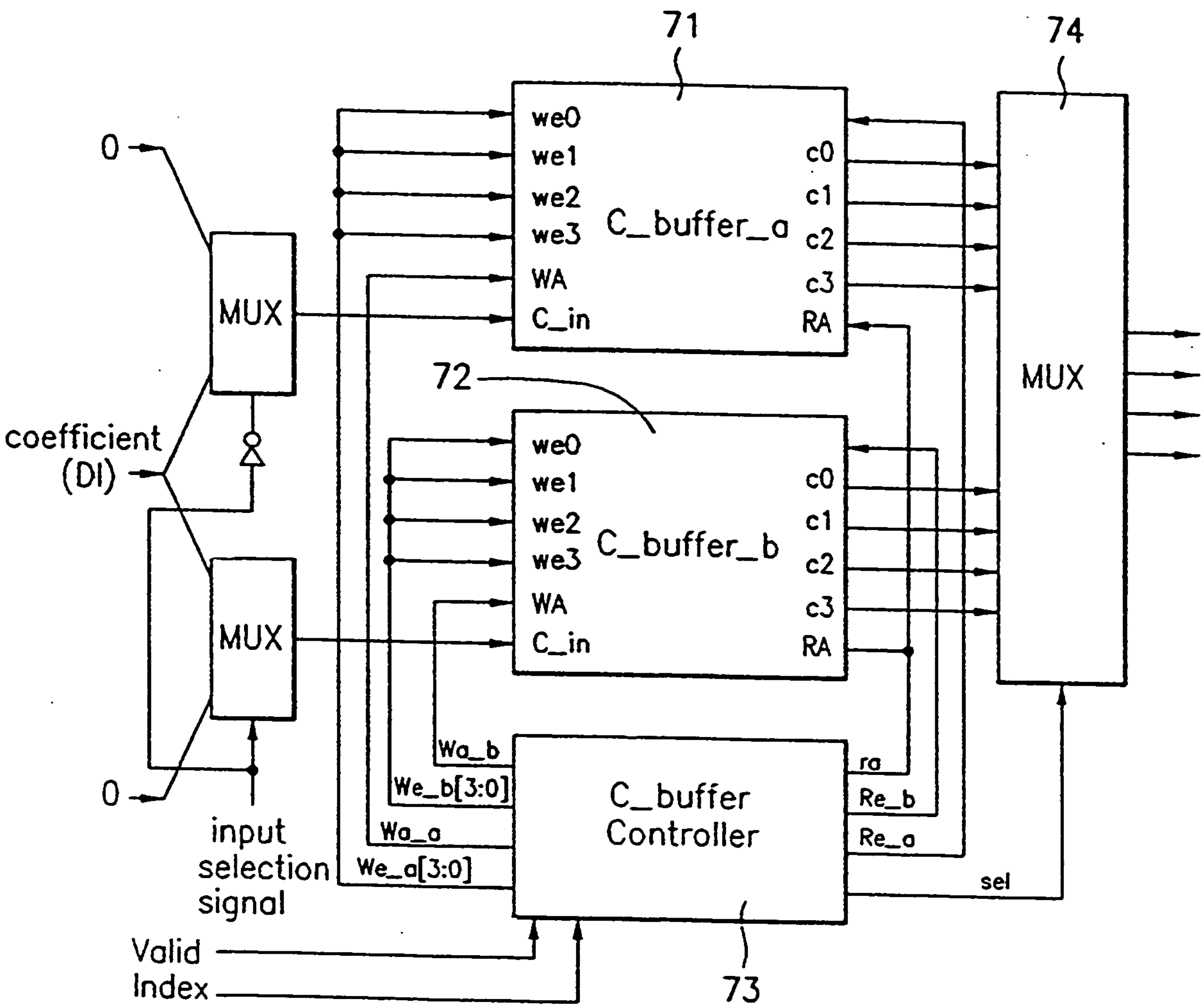

(a) clock
(b) start(I)
(c) end(I)
(d) valid(I)
(e) run(I)
0 3 2 6 8 0 9
(f) level(I)
125 −11 4 −1 5 1 −2
(g) start(O)
(h) end(O)
(i) valid(O)
(j) index(O)
0 4 7 14 23 24 34
(k) level(O)
125 −11 4 −1 5 1 −2

FIG.6



Quantization level
63
level
DCT
coefficient(coef)
q_m
Index
Address
Converter
Read
Address
Quantization
matrix
61
62

FIG.7



71
74
0
MUX
we0
we1
we2
we3
WA
C_in
C_buffer_a
c0
c1
c2
c3
RA
MUX
72
coefficient
(DI)
we0
we1
we2
we3
WA
C_in
C_buffer_b
c0
c1
c2
c3
RA
MUX
0
input
selection
signal
Wa_b
We_b[3:0]
Wa_a
We_a[3:0]
C_buffer
Controller
ra
Re_b
Re_a
sel
Valid
Index
73

FIG.8

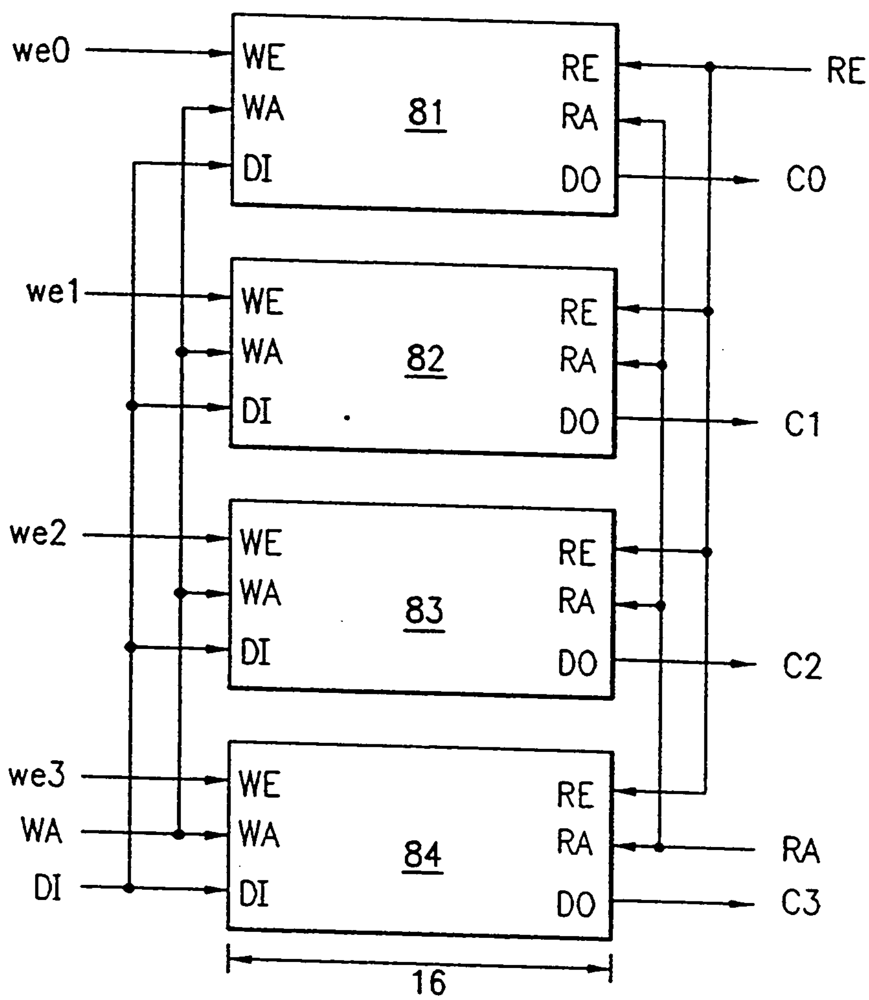

we0
we1
we2
we3
WA
DI
WE
WA
DI
81
82
83
84
RE
RA
DO
RE
C0
C1
C2
RA
C3
16

FIG.9

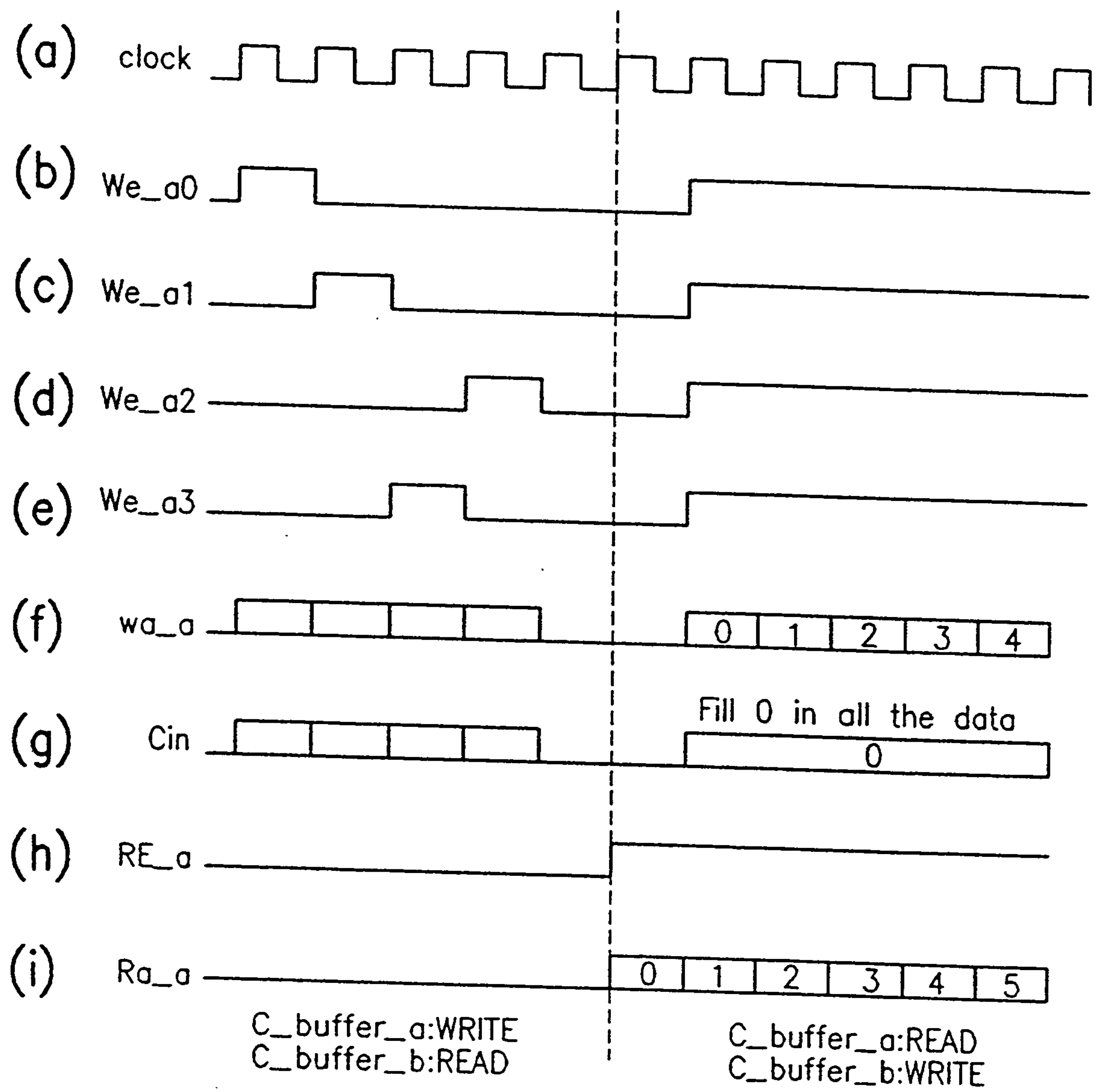
1	2	6	7	15	16	28	29
3	5	8	14	17	27	30	43
4	9	13	18	26	31	42	44
10	12	19	25	32	41	45	54
11	20	24	33	40	46	53	55
21	23	34	39	47	52	56	61
22	35	38	48	51	57	60	62
36	37	49	50	58	59	63	64

WA

We

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	11	2	20	6	24									29	55
1	3	21	5	23	8	34									43	61
2	4	22	9	35	13	38									44	62
3	10	36	12	37	19	49									54	64

FIG.10


(a) clock
(b) We_a0
(c) We_a1
(d) We_a2
(e) We_a3
(f) wa_a
0 1 2 3 4
(g) Cin
Fill 0 in all the data
0
(h) RE_a
(i) Ra_a
0 1 2 3 4 5
C_buffer_a:WRITE
C_buffer_b:READ
C_buffer_a:READ
C_buffer_b:WRITE

VIDEO DECODER FOR HIGH PICTURE QUALITY

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a device which performs inverse quantization and inverse scanning at high speeds in a high picture quality video decoder for high definition television.

Discussion of Related Art

In recent years, digital television (TV) broadcasting has been drawing much attention, and much research and development are now devoted to techniques of compressing and transmitting video data to enjoy the screen of high picture quality through televisions. The moving picture experts group-2 (MPEG-2) is normally used as algorithm for compressing video signals, and the compression rate is 1/40 to 1/60. Such algorithm is used to transmit digital data of high picture quality via general broadcasting channel. The digital TV receiver requires a video decoder for recovering the compressed input video data into

original high picture quality video data. The video decoder for digital broadcasting must have a data processing rate 5 or 6 times as high as common-type video decoders' in order to decode video signals of high picture quality.

FIG. 1 is a block diagram of a conventional video decoder which is used to process video signals of general resolution whose volume is 15MByte per sec.

A video bit stream applied from an encoder is decoded in a variable length decoder (VLD) 11 to be divided into motion vector, quantization value, DCT coefficient.

A value corresponding to the DCT coefficient of VLD 11's output is input to inverse discrete cosine transformer (IDCT) 14 through inverse scanner (IS) 12 and inverse quantizer (IQ) 13. VLD 11 decodes the DCT coefficient into a run-level pair. That is, a single DCT block is formed of coefficients of 8 x 8, and only coefficients not 0 of them are in a code. So, VLD 11 produces a level and a run as to the size of coefficients not 0, i.e. how many 0s are inserted between these coefficients.

If the first, fourth, second and third ones of 64 coefficients are 10, 3, 0, and 0, run-level is (0,10) and (3,3). This should be decoded to 10, 0, 0, 0, 3, and as shown

in FIG. 2, a run-level decoder 21 is needed to change run-level pairs to 64 consecutive DCT coefficients. As shown in FIG. 3a, the decoding of 8 x 8 coefficients is in zigzag order so as to begin with low frequency signals in transfer to enhance the run-level code, and as shown in FIG. 3b, it is changed to a raster scanning method before IDCT 14 performs IDCT. In order to do this, as shown in FIG. 2, a memory 22 for temporarily storing DCT coefficients and an address controller 23 for providing a read/write address to memory 23 are required. Inverse scanning is carried out by changing the read/write address. Memory 22 and address controller 23 correspond to inverse scanner 12 of FIG. 1. IQ 13 performs an inverse quantization with respect to 64 DCT coefficients produced from inverse scanner 12 after inverse scanning according to the quantization value, and produces its output to IDCT 14.

IDCT 14 performs an IDCT with respect to the DCT coefficients inversely quantized to produce its output to a motion compensator 15. Motion compensator 15 recovers the output of IDCT 14 to a complete image by using the video signal inversely discrete cosine transformed and the motion vector separated in VLD 11, and outputs the image to display

16.

Display 16 rearranges data according to a picture type before producing, or outputs the data directly. The video decoder system based on MPEG-2 employs an external memory such as dynamic random access memory 22, and DRAM 22's blocks are divided into read of required data, write of data motion compensated and read of data to be displayed for read/write of the bit stream and motion compensation. Thus, each block of FIG. 1 has first input first output (FIFO) parts 17 to 20, and transfers and receives data via memory controller 21.

The common-type video decoder is used for processing a small volume of data but is not suitable for processing a large volume of data. That is, since the data volume is increased by six times in order to decode video data of MPEG-2 MP@HL, data of more than 93 MBytes per sec. must be processed, and each component has a processing rate six times as fast as the common-type video decoder of FIG. 1. In addition, the memory size and the data transfer rate used therefor must be increased.

Most DCT coefficients of the compressed bit stream are zero, and while VLD 11 requires 5 to 6 clocks to decode a single block, **run-level decoder 21, producing 64 DCT

coefficients, needs 64 clocks. Therefore, VLD 11 is in idle mode when run-level decoder 21 is operating, which is inefficient.

If such a structure is applied to an HDTV, the VLD, the run-level decoder, the inverse scanner, the IQ should operate at clocks of 94MHz, which applies heavy load to the hardware since the clock frequency is too high, and enables decoding. The inverse scanning using this structure can be performed in serial only, and the internal memory write and read speeds should be very high.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a video decoder for high picture quality that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

Preferred embodiments of the invention provide a video decoder for high picture quality which can perform a parallel processing when needing high-speed performance, and can consecutively process video data for a given period of time.

Additional features and advantages of the invention will be set forth in the description which follows, and in part

will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

According to the present invention there is provided a video decoder for high definition television including a variable length decoder decoding codes corresponding to discrete cosine transform (DCT) coefficients of an applied video bit stream, and producing a run-level pair for each code; an index decoder storing run-level pairs produced from the variable length decoder, and producing the position information indicating the number of a level value of a corresponding run-level pair among 64 DCT coefficients; an inverse quantizer obtaining an added value corresponding to the position information of the index decoder from a quantization matrix, and performing an inverse quantization by multiplying a quantizer level for determining a quantization step and DCT coefficient to the added value; an inverse scanner including a plurality of memories, and inversely scanning the DCT coefficient inversely

quantized and applied serially from the inverse quantizer and producing the DCT coefficient in parallel at the same time; and an inverse discrete cosine transformer performing an inverse discrete cosine transformation (IDCT) of the DCT coefficient produced in parallel from the inverse scanner.

In one embodiment the video decoder includes first and second buffers that each consist of a plurality of memories and selectively write applied data into the memories by providing a different write enable signal to each memory while commonly providing data and write address to the plural memories, and commonly applies the read address and read enable signal to a plurality of the memories, thus reading data out of the memories at the same time, and producing the data in parallel. The buffer controller generates a write/read address and a write/read enable signal of the memories by using valid and index signals to write the inversely quantized DCT coefficients into a plurality of the memories one by one, and to simultaneously read the DCT coefficients from the memories.

The buffer controller generates the write/read address and the write enable signal to write 0 into a position where the data is read, simultaneously with reading the data from

one coefficient buffer. When reading data from one coefficient buffer, 64 DCT coefficients with 0 that have been already written are all read out.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the drawings:

In the drawings:

FIG. 1 is a block diagram of a video decoder in accordance with a conventional art;

FIG. 2 is a block diagram for run-level decoding and inverse scanning of FIG. 1;

FIGS. 3a and 3b depict a zigzag scanning and a raster scanning, respectively;

FIG. 4 is a block diagram of a video decoder for high

picture quality in accordance with the present invention;

FIGS. 5a to 5k each depict input/output waveforms of FIG. 4's index decoder;

FIG. 6 is a detailed block diagram of an inverse quantizer (IQ) of FIG. 4;

FIG. 7 is a detailed block diagram of a coefficient buffer of FIG. 4;

FIG. 8 is a detailed block diagram of FIG. 7's buffer;

FIG. 9 depicts the inverse scan address generation; and

FIGS. 10a to 10i are read/write timing charts of the coefficient buffer.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. 4 is a block diagram of a video decoder for high picture quality in accordance with the present invention. A VLD 41 that separates motion vector, quantization value, DCT coefficients from a video bit stream to produce a run-level pair; an index decoder 42 which stores run-level pairs output from VLD 41 and produces an index indicative of the number of

the level of each run-level pair among 64 coefficients; an IQ 43 performing IQ using the index and the level of index decoder 42; a coefficient buffer 44 producing DCT coefficients serially applied from index decoder 42 and performing an inverse scanning at the same time; and an IDCT 45 performing an IDCT with respect to DCT coefficients applied in parallel.

In the illustrated embodiment DCT coefficients serially produced from VLD 41 are converted to be applied to IDCT 45, and the inverse quantization and the inverse scanning are performed. VLD 41 decodes codes corresponding to DCT coefficients of the video bit stream, and produces a run and a level for each code. This run-level value has the following meaning: (run, level) ------ 0's with number of run, one level

[ex. 1] (0,23) ------ 23

[ex. 2] (5,8) ------ 0,0,0,0,0,8

There are 64 coefficients (= 8 x 8) with respect to a single DCT block, and since each code consists of a run-level, run-level pairs produced from a single block are produced by the number of coefficients not 0. For reference, since most DCT coefficients are 0, the run-level pairs generated per block are less than 20 on the average. Such run-level pairs must be converted into DCT coefficients including 64 0's, and

the output by the run-level is carried out by zig-zag scanning, as shown in FIG. 3. These coefficients are rearranged in IDCT 45, which is inverse scanning.

The run value of the run-level pairs output from VLD 41 is stored in index decoder 42. Index decoder 42 produces an index indicative of the number of the level of a run-level pair among 64 coefficients. Therefore, this index is one of 0 to 63.

FIGS. 5a to 5k are input/output wave forms of index decoder 42, and while FIGS. 5a to 5f concern signals applied to index decoder 42, FIGS. 5g to 5k relate to signals output from index decoder 42. When VLD 41 generates a start pulse of FIG. 5b synchronized with a clock of FIG. 5a, a valid signal goes 'high' as shown in FIG. 5d, and run-level pairs are produced as depicted in FIGS. 5e and 5f. Once an end pulse is generated, the valid signal goes 'low', and run-level pairs are not produced. Index decoder 42 produces signals similarly, as shown in FIGS. 5g to 5k, and its run and index values are a little different from the above. That is, the run value is indicative of the number of 0's between coefficients not 0, and index value is indicative of the number of the level value among the 64 coefficients.

The output DCT coefficients are applied to IQ 43. IQ 43 multiplies a quantizer level value and quantization matrix to the respective DCT coefficients. The quantizer level is multiplied to the respective 64 coefficients equally, and the value of the quantization matrix is different according to the 8 x 8 position of the DCT coefficients. Therefore, the position of corresponding one of the coefficients should be found.

IQ 43 reads an added value of a corresponding position in the quantization matrix from the applied index, and multiplies it to the DCT coefficient.

FIG. 6 is a detailed block diagram of IQ 43, and IQ 43 includes an address converter 61 that converts the index into a read address of the quantization matrix, a memory 62 storing the quantization matrix, and a multiplier 63 multiplying the quantizer level, a level value decoded by VLD 41, and the quantization matrix.

Address converter 61 is used to convert indexes in zzigzagzag order into those in order of quantization matrix memory 62 stored by raster scanning, and multiplier 63 multiplies memory 62's output qm read from the read address generated from address converter 61, the quantizer level,

level value produced through index decoder 42, thus producing DCT coefficients coef that will be used as inputs of IDCT 45. IQ 43 produces start, end, valid, and index signals except DCT coefficients coef. The DCT coefficients produced from IQ 43 are converted in parallel to enhance the processing rate, and simultaneously applied to coefficient buffer 44. IQ 43 produces coefficients not zero so the volume of its output data is not large, and if 0 is added thereto to be produced to IDCT 45, the volume of data is significantly increased. Thus, when the data is not processed in parallel, high-level clocks are used for the very high processing rate, and heavy load is applied to the hardware. The clock speed can be lowered by processing the 64 coefficients with zero, and in order to do this, coefficient buffer 44 changes data in parallel and performs an inverse scanning by using four memories in parallel.

FIG. 7 is a block diagram of coefficient buffer 44, and buffer 44 includes a first buffer 71 storing coefficients, a second buffer 72, a coefficient buffer controller 73 generating read/write address and read/write enable signals, and a multiplexer 74 selectively producing output data of buffer 44. Two buffers 71 and 72 are used to store

coefficients, and coefficients of one block are written in one of them while the previous block is read out of the other buffer. They take their turns in reading and writing for writing the next block. The write address and read address are produced from buffer controller 73. Each one of coefficients is written into the respective four memories of each buffer, and four coefficients each written into four memories are simultaneously read, thus producing serially applied data in parallel. Write enable signals we_a[3:0], and write addresses wa_a,wa_b are produced by using the valid and index signals.

FIG. 8 is a detailed block diagram of FIG. 7's first and second buffers 71 and 72, and each buffer includes four memories 81 to 84. Applied data DI and write address WA are connected in common to four memories 81 to 84. Write enable signals we0, we1, we2, and we3 are each connected to four memories 81 to 84 so writing into the memories is selectively performed. Read address RA is commonly connected to the memories so reading from four memories 81 to 84 is simultaneously performed.

A method of generating address and enable signals from buffer controller 73 is as follows. Basically, when writing a DCT coefficient into one coefficient buffer, the other

coefficient buffer inserts 0 in a position from which data has been already read, simultaneously with reading already written DCT coefficients, so there is no need to purposely insert 0 into the memory prior to writing of the next block. Each buffer 71 and 72 consists of four memories for storing data of 8 x 8 blocks divided into four. Buffer controller 73 detects the position of the DCT coefficient applied by using the index signal produced from IQ 43, and determines into which one of four memories and into which address the DCT coefficient is written and writes corresponding memory's address, thus performing inverse scanning.

FIG. 9 shows a method of converting the index signal from IQ 43 into the coefficient buffer's address. To read the index signals, applied in zigzag scanning order, in raster scanning, indexes of the respective coefficient are divided into WA and We and converted. If index is 23, signal we1 of the corresponding buffer is enabled, and 5, a DCT coefficient, is written into a fourth address (WA = 3) of memory 82 enabled by signal we1. Since the value other than the written data has been already filled with 0, all the 64 coefficients can be read out.

FIGS. 10a to 10i are timing charts of signals controlling

first buffer 71 of two buffers, and two buffers 71 and 72 take their turns in reading and writing. The signals are generated from write address wa_a for writing, and 16 data are consecutively read out per block for reading. A write address and write enable signal are generated in the position of the read data so as to write 0 at the next clock. That is, when writing data into first buffer 71, data is read from second buffer 72, and when writing data into second buffer 72, data is read from first buffer 71. The buffer reading the data writes 0 in the position where the data is read out. That is, reading is performed in one buffer 71 or 72, and write can be performed in both buffers 71 and 72. Outputs of first and second buffers 71 and 72 are selected by multiplexer 74, and are transmitted to IDCT 45 by four coefficients. IDCT 45 performs an inverse IDCT in the unit of 8 x 8. The MPEG standards propose two-dimensional IDCT of 8 x 8 block. One dimensional IDCT with respect to the applied data is performed, and after column-row preposition, one-dimensional IDCT is performed, thereby completing 8 x 8 two-dimensional IDCT. Coefficients produced from VLD 41 are converted into parallel data filled with 0 to be applied to IDCT 45 as the IQ and inverse scanning are performed, so the high speed data

processing can be assured.

When the present invention is embodied in a video decoder for high definition television requiring the data processing volume and processing rate, IQ/inverse scanning/IDCT can be performed at high speed with the VLD operating at low speed. In conclusion, the described embodiment can reduce circuits and is realized with appropriate clocks compared to a conventional video decoder, and the video decoder can be integrated in one integrated circuit.

The processing time can be reduced because there is no need to perform IQ with respect to 0 by performing IQ with the position information on the 8 x 8 block of the coefficient decoded from a given run without producing 0 by using the run-level decoder with respect to the run-level of the coefficient decoded after VLD.

In addition, serial data can be converted into parallel data simultaneously with performing the inverse scanning by producing the write address of the coefficient memory arranged in parallel by using the position information of coefficients from the VLD with storing the inversely quantized DCT coefficient in the memory, so the clock rate may be decreased not to apply heavy load to the hardware.

64 coefficients with 0 can be all produced by the use of only coefficients not zero by inserting 0 into the memory prior to writing coefficients not 0 into the memory for generating 64 coefficients per block, thus increasing the processing rate.

It will be apparent to those skilled in the art that various modifications and variations can be made in the video decoder **described** ———————— without departing from the ———— scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims.

What is claimed is:

1. A video decoder for high definition television comprising:

a variable length decoder decoding codes corresponding to discrete cosine transform (DCT) coefficients of an applied video bit stream, and producing a run-level pair for each code;

an index decoder storing run-level pairs produced from the variable length decoder, and producing the position information indicating the number of a level value of a corresponding run-level pair among 64 DCT coefficients;

an inverse quantizer obtaining an added value corresponding to the position information of the index decoder from a quantization matrix, and performing an inverse quantization by multiplying a quantizer level for determining a quantization step and DCT coefficient to the added value;

an inverse scanner including a plurality of memories, and inversely scanning the DCT coefficient inversely quantized and applied serially from the inverse quantizer and producing the DCT coefficient in parallel at the same time; and

an inverse discrete cosine transformer performing an inverse discrete cosine transformation (IDCT) of the DCT coefficient produced in parallel from the inverse scanner.

2. A video decoder according to claim 1, wherein the inverse quantizer includes:

an address converter converting the position information produced from the index decoder into a read address of the quantization matrix;

a memory storing the quantization matrix and producing a quantization matrix added value in the read address produced from the address converter; and

a multiplier multiplying a quantization level determining the quantization step, the DCT coefficient produced through the index decoder, and quantization matrix added value produced from the memory.

3. A video decoder according to claim 2, wherein the address converter converts the position information in zigzag scanning order into data in order of the memory stored by raster scanning.

4. A video decoder according to claim 1, wherein the inverse scanner finds the position of the DCT coefficient inversely quantized by using the applied position information signal, and performs an inverse scanning by a corresponding address of a corresponding one of plural memories.

5. A video decoder according to claim 1, wherein the inverse scanner includes:

first and second buffers storing the DCT coefficient inversely quantized;

a coefficient buffer controller generating a write/read address and a write/read enable signal to the first and second buffers; and

a multiplexer selectively producing output data of the first and second buffers to the inverse discrete cosine transformer.

6. A video decoder according to claim 5, wherein when one of the first and second buffers is writing coefficients of the current block, the other buffer reads the previous block, and if completing the writing and reading, they take their turns in writing and reading.

7. A video decoder according to claim 5, wherein the first and second buffers each consist of a plurality of memories and selectively write applied data into the memories by providing a different write enable signal to each memory while commonly providing data and write address to the plural memories, and commonly applies the read address and read enable signal to a plurality of the memories, thus reading data out of the memories at the same time, and producing the data in parallel.

8. A video decoder according to claim 5, wherein the buffer controller generates a write/read address and a write/read enable signal of the memories by using valid and index signals to write the inversely quantized DCT coefficients into a plurality of the memories one by one, and to simultaneously read the DCT coefficients from the memories.

9. A video decoder according to claim 5, wherein the buffer controller generates the write/read address and the write enable signal to write 0 into a position where the data is read, simultaneously with reading the data from one coefficient buffer.

10. A video decoder according to claim 5, wherein when reading data from one coefficient buffer, 64 DCT coefficients with 0 that have been already written are all read out.

11. **A video decoder substantially as herein described with reference to Figures 4** to **10i of the accompanying drawings.**

Application No: GB 9828722.0
Claims searched: 1 to 11

Examiner: John Donaldson
Date of search: 10 May 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H4F(FRR, FRW)

Int Cl (Ed.6): H04N 7/00, 7/015, 7/24, 7/26, 7/30, 7/32, 7/48, 7/50, 11/00, 11/02, 11/04

Other: Online:WPI, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	EP 0149121 A2 (IBM), see abstract	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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